6.3: Fast Addressing of Plasma Display Panels

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Abstract
The dynamics of the address discharge and the mechanism behind it are being analyzed. Based on this analysis a novel addressing waveform using low-voltage addressing drivers and leading to a significant reduction of the overall panel addressing time is being proposed. 3D PIC/Monte-Carlo simulations of the address discharge in a PDP cell have shown that for certain cell geometries the addressing time of up to 600-800ns per line can be achieved.

1. Introduction
With recent improvements of plasma displays, switching to a high-definition (HD) and 10-subfield addressing the addressing time has become a critical issue. Indeed, if it takes ~2μs to address a line, then for 10-subfield addressing scheme it will take ~7.5-10*ms* (768-1080 lines) for addressing the panel using dual-scan method. If one adds 2-4*ms* for the ramp reset time, then the time left for the actual sustaining will be only about 2-6*ms*. While 6*ms* may be marginally satisfactory, less than 6*ms* is certainly not enough time for sustaining and have a bright display. This creates a serious problem, which currently is being resolved by using interlacing, variable sustain frequency, complex algorithms instead of a true 10-subfield scheme, etc. In the result, new artifacts appear, and while new panels do not have distortions that older 8-subfield panels had, the quality of a static image of new HD and especially Full HD panels are often worse than of older ones with lower number of subfields. Thus, the addressing speed has become a bottleneck for a high quality panel.

The addressing of a PDP was approached earlier from different perspectives - reliability, speed and contrast, but none of the proposed methods satisfies all requirements acceptable for a high quality HD display. Since the image quality is a "must" for HD TV we will discuss here only methods that provide high contrast of the image, or employ the ramp reset waveform [1]. We discussed earlier in details the operation of the ramp discharge [2], and correct reset waveform [3]. The important feature of this setup (besides of a low background light) is that one can control somewhat the wall charge and set a cell in a specific state minimizing the address voltage. Later Sakita et al. [4] and Kim et al. [5] introduced a concept of a VT-close curve, which helps designing the ramps setup in a three electrode system. They concluded that if at the end of the ramp each cell reached the state that corresponds to simultaneous discharges between scan electrode and two other electrodes and is positioned in the appropriate corner of the VT-close curve, then it would lead to the easiest addressing – the address pulse will appear even with a relatively low addressing voltage.

In this report we propose a new method of addressing plasma display panels [6]. Based on our investigation of charged particles motion in a cell, we analyzed the mechanism of the address discharge initiation and found that there is a possibility of having address discharges simultaneously in two or more lines, thus shortening the **overall** address period rather than address discharge in each individual cell.

2. Conventional addressing
To understand the idea of new addressing let us first characterize a common selective addressing scheme, shown schematically in the Fig.1, starting with the reset period. First, the ramp reset is applied to the whole panel. At the end of this period, when every cell experiences discharges both between sustain and between scan and address electrodes, the positive voltage V_{lock} is applied to all scan electrodes, interrupting discharges in every cell, washing out charged particles, and preventing cells from being fired when the address voltage V_{ON} is applied to address electrodes. For future reference we will call this - "locking" the panel. Then selective addressing can be described as the following sequence of actions: **"unlock the line → address the "ON" cells → lock the line →go to the next line"**. Locking the row after addressing the line prevents misaddressing of the "OFF" cells, when later on cells in the same column but in different rows are addressed "ON".

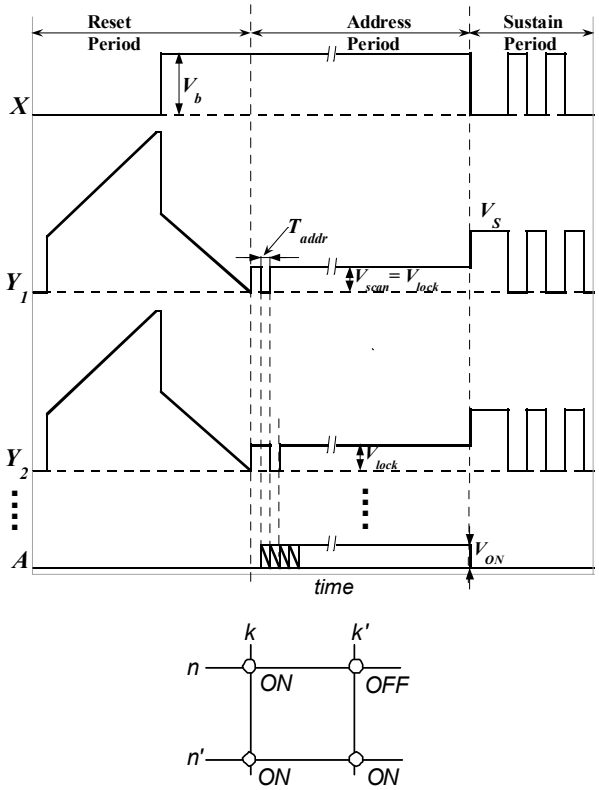

Figure 1. Conventional driving scheme. Three periods (reset/ setup, address and sustain) are present. Locking the row after addressing prevents "OFF" cells *(n,k')* of the addressed row *n* from being ignited, when the cell *(n',k')* of the other row *n'* is being addressed "ON" later on. ***X*** and ***Y*** designate bulk and scan sustain electrodes, and ***A*** – the data electrode.

Although even low address voltage (V_{ON}) can address the cell when one uses the suggested by Sakita et al. rule, the addressing time may be quite large, so one has to use rather large voltage V_{ON}

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to accelerate the initiation of the discharge. Another factor restricting the address time is the possibility of reducing the memory charge and even of a secondary discharge, erasing memory charge if the scan pulse ends before the charge particle density in the cell drops to a low enough magnitude. The last factor worth mentioning relates to both conventional driving scheme and common choice of geometrical parameters of a PDP cell – they both promote long statistical delays of the address discharge.

3. New addressing scheme

3.1 Initiation of the Address Discharge

When (during the address period) the scan voltage is applied to the ***Y*** electrode, it brings row to the same condition it was in the end of the reset period, when the voltage between both pairs of electrodes ***Y-A*** and ***Y-X*** are equal or close to the appropriate breakdown one. So, if one applies positive voltage to the address electrode, it initiates ***Y-A*** discharge across the Plate Gap (PG) between address and scan electrodes. This discharge by itself does not produce large memory charge on the dielectric over the scan electrode. The primary function of the PG discharge, though, is to initiate the strong ***Y-X*** Sustain Gap (SG) discharge between the scan ***Y*** and the bulk ***X*** sustain electrodes, which transfers large charge between them. This discharge between ***X*** and ***Y*** electrodes is the one responsible for the memory charge required for further sustaining of the cell. The mechanism of initiation of the SG discharge depends on geometrical parameters of the cell and voltages between electrodes. To shorten the address time one usually increases the amplitude of the address voltage and shortens the gap between ***X*** and ***Y*** electrodes. Such way stimulates electron diffusion from the growing PG discharge into the region of SG discharge, which at some level of electron source becomes unstable and strong SG discharge develops in the cell. High density plasma produced during this discharge, stays in the cell well after the current has decayed. If one tried to lock the line back again and changed the voltage applied to the scan electrode too early, while the plasma density was still high, it could result in erasing the memory charge.

3.2 Dual Addressing Scheme

This simple scheme is rugged enough to work in any panel, but ignores the possibility of faster addressing if one exploits some important features of the address discharge. One of these features is that once the strong SG discharge started it would continue, even if the voltage applied to the data electrode is changed or even completely removed. In fact, it may even slightly increase the memory charge. So, if one started addressing the next row (unlock and apply appropriate address voltages) **without locking the current one**, it would not affect in a negative way the memory charge of the cells addressed "ON". It will, however, produce undesirable "ON" discharges in the "OFF" cells that were not addressed previously, which would result in misaddressing. One can, though, generate in the "OFF" cells additional erasing PG discharges, which transfer enough charge across the plate gap to make impossible misaddressing of those cells later on when higher "ON" voltage is applied to the same data electrodes.

The new selective addressing is shown in Fig.2 and can be described by the following sequence: **"unlock the row → address both "ON" and "OFF" cells → go to the next row"**. The time between unlocking two subsequent lines is limited by the time of the "OFF" discharge, which can be made significantly faster than the "ON" discharge, if it is initiated only across a short plate gap, and does not have the long inertial part related to plasma decay in the afterglow of a strong "ON" discharge. As shown in the Fig. 2, the voltage V_{OFF} initiating the "OFF" discharges is applied to **all** data electrodes (or "$-V_{OFF}$" to **all** sustain electrodes) in the beginning of the address period for the duration of the whole period, so that address drivers have to control only the additional voltage $V_{addr} = V_{ON} - V_{OFF}$ necessary to apply on top of V_{OFF} to selectively address "ON" cells, and "OFF" cells are in a way addressed by the scan electrode. That is why we name it the "**Dual Addressing**". To make the "OFF" discharge faster, one should have the voltage V_{OFF} as high as possible. We will discuss this issue below, here let just mention that one has to prevent the "OFF" discharge from initiating the SG discharge, so one may have to obstruct such initiation by creating a barrier for electron diffusion by applying V_{Xlock} to the bulk sustain electrode (Fig.2).

"The next" line or row means the next in sequence, and it does not have to be the neighboring row. As a matter of fact the best sequence is probably similar to a dual or triple scan sequences: (*1, N/2+1, 2, N/2+2, 3, N/2+3, ...*) or *(1, N/3+1, 2N/3+1, 2, N/3+2, 2N/3+2, 3, N/3+3, 2N/3+3,…)* , where ***N*** is the total number of rows controlled by a particular scan driver.

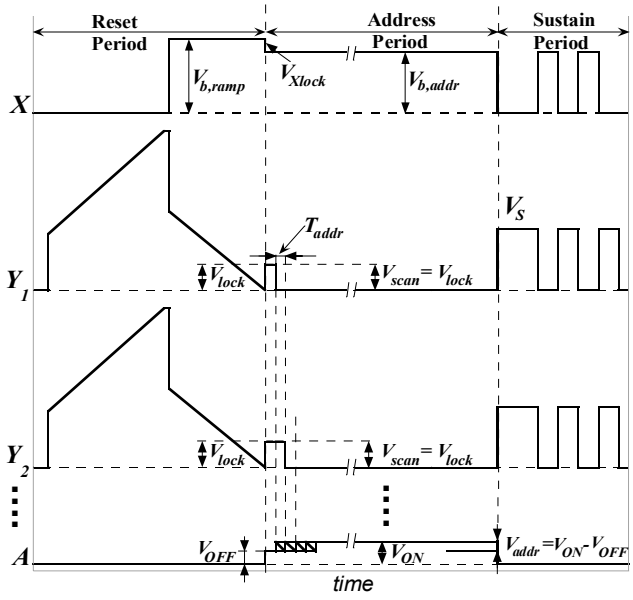

Figure 2. Dual addressing scheme. In the beginning of address period the panel is locked by V_{lock}, applied to ***Y*** electrodes. Additionally for the whole addressing period voltage V_{OFF} is applied to all data electrodes, and barrier voltage V_{Xlock} is applied to all ***X*** (bulk) sustain electrodes. Unlocking the raw automatically addresses "OFF" cells, while the address voltage applied to selected data electrodes (on top of V_{OFF}) addresses "ON" cells. Addressing the next row starts as soon as "OFF" discharge is complete, and the line stays unlocked till the end of the address period.

The proposed addressing scheme will work only if one can realize the fast "OFF" discharge without starting strong discharge between sustain electrodes, and this is not always possible. There are few factors that one has to take into account. The main two are the discharge priming and the mechanism of the initiation of the discharge between sustain electrodes, which depends on geometrical parameters of the cell and applied voltages.

With regard to the priming, one should not expect any charged particles or metastables in the gap left after the ramp discharge - they all disappear from the gap in time much shorter than the address period and for the most of the panel these sources do not exist. Also we will not assume that there is any reliable priming coming from the previously addressed neighboring rows - as we already mentioned we want to consider possibilities of different addressing sequences. We assume though, that there is a weak source of electrons due to exoemission, however strong enough to guarantee the stable operation of the ramp discharge. Anyway, the priming is a separate issue, which plays equally important role in any addressing scheme.

The second factor is unique to this method of addressing. In order to operate with large voltage V_{OFF} and small V_{addr} and have reliable addressing one needs to separate sustain and plate gap discharges better than diffusive addressing provides. One can use the barrier voltage V_{Xlock} up to some limit, but the best way is to change geometrical parameters of the cell. For example, if one uses very wide sustain gap then PG and SG discharges can be well separated even without additional voltage barrier V_{Xlock}. Instead of diffusive addressing that we described before we suggest to use two different modes of plate gap discharge for the "OFF" and "ON" discharges – weak and strong. Weak mode [7] does not lead to large plasma density and to significant distortion of electric field, so the only way it affects the condition in the sustain gap is through diffusion, which can be suppressed. The strong mode [8] produces high density plasma which strongly affects the electric field, and will completely change conditions for initiating the SG discharge. The advantage of such addressing lies in the fact that only a few additional Volts applied to a gap will change one mode to another, thus making possible low voltage addressing. Using common geometry with sustain gap around 70-120 μm and plate gap around 90-130 μm we were not able to separate these discharges and realize the proposed scheme to the full extent (sub-microsecond addressing of a line), because electron diffusion in such geometry makes interaction between them too strong. The main advantage in that case was lower addressing voltage. However when we used larger sustain gap (260 μm and more), smaller plate gap (70-80 μm) and new (proprietary) ramp waveform we were able to fully realize this idea with only 10V for addressing.

Two additional advantages of the new method and this geometry are short statistical and formative delays of the discharge. The formative delay is shorter because the length of the field lines along which the "OFF" discharge develops L, is shorter than in a regular PDP cell, and formative delay depends on it as L^{-2}. The statistical delay is much shorter since it also depends on the discharge structure, and this one is advantageous compared to a discharge in a regular cell. In all simulations referred below we used 86%Ne+14%Xe mixture, and used γ_{Ne} = 0.64, γ_{Xe} = 0.01 for the vacuum values of the secondary emission coefficients. All simulations were made using 3D Particle-In-Cell/Monte-Carlo kinetic code.

3.3 Numerical Results (3D PIC/Monte-Carlo)

The Table 1 shows the voltage transferred in the OFF discharge between scan and data electrodes as a function of the amplitude of the address voltage for the "OFF" discharge obtained in 3D Particle-In-Cell simulation of the discharge in the cell with plate gap of 70μm, and sustain gap of 260μm. Table also contains half-width of the discharge pulse, the width between moments when the number of ions in the gap is 5000, the peak amount of ions in the gap, the total time for the discharge in our simulation (including the ramp time of 100ns that we used to apply the voltage) taken at the moment when the current dropped to 20% of its peak value. One can see that 40-50V for the V_{OFF} will guarantee that the whole time for the discharge will be around 600-700ns for the exoemission rate of 20 electrons per microsecond from the whole cathode. This rate is already low to support a stable ramp, but even if one adds another 100ns to the total time for extra bad cell one will still be within 1μs time per line. One should add that if one uses higher voltage V_{OFF}, than one can move to the next line even before the discharge ends, since the necessary charge has already being transferred. One can see from the Table 1, that addressing "ON" voltage (V_{addr}) is only 10V. In these simulations we used V_{Xlock}=0.

Table 1

Parameter / V_a	30V	40V	50V	60V
ΔV_{gap}, V	62	70	102	Break (ON)
$\tau_{1/2}$, ns	270	155	118	xx
$T(5000)$, ns	895	810	747	xx
$N_{i,max}(10^5)$	6.55	15	27.9	xx
T_{tot}, ns	770	680	472	xx

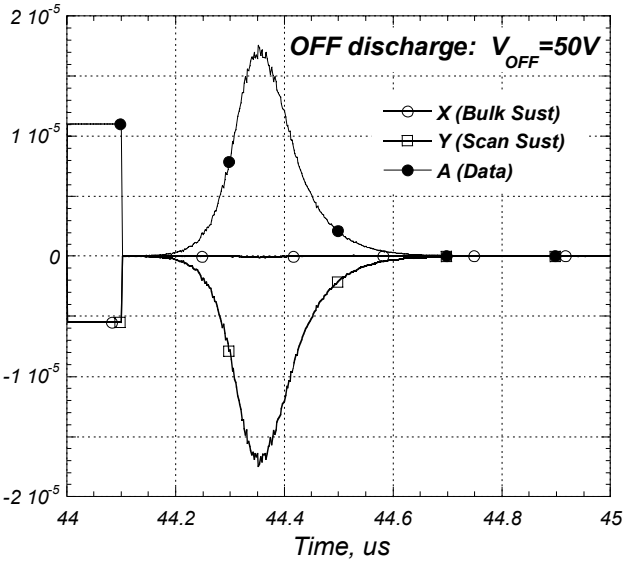

Figure 3. Current through electrodes during the select "OFF" discharge for the case of V_{OFF} =50V.

From the Fig. 3, which shows currents during discharge with V_{OFF} =50V one can see that the third electrode is practically not involved at all, which means that sustain and plate gap discharges are separated completely.

Figure 4 shows the plot of the number of ions in the gap for the same discharge (V_{OFF} =50V) from which one can see that as soon as first electrons appear in the gap (initially without ANY charged particles) the number of ions grows to a few thousand in just about 100ns. After their number reaches about 2000 -3000 it growth exponentially (with characteristic time $\tau \sim$ 14.5ns) following the fluid theory [7].

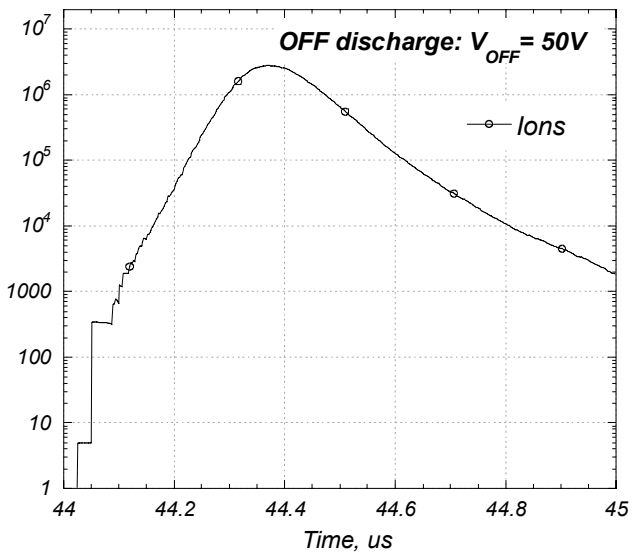

Figure 4. Number of ions in the gap during the "OFF" discharge for the case of V_{OFF}=50V.

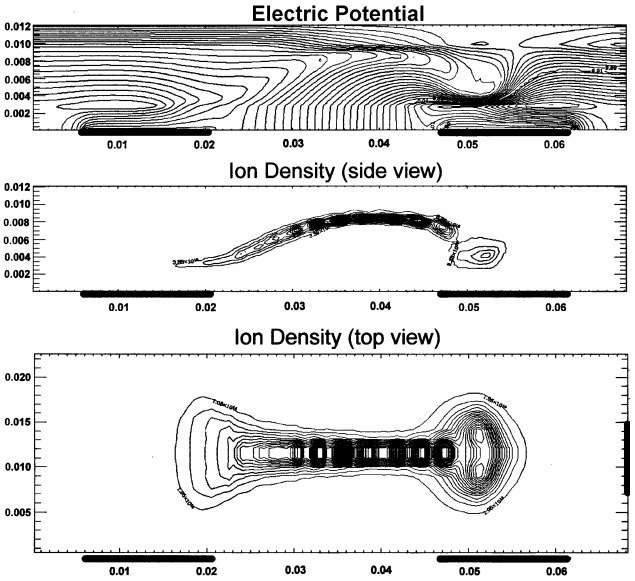

Figure 5. Equipotential lines, and the ion density ("top" and "side" views) after the beginning of the discharge (330ns) for the case of V_{addr}=10V (V_{ON}=60V).

Figure 5 shows the "ON" discharge initiated by a 10V address pulse (V_{ON}=60V) after just about 330ns after the beginning. One can see well developed discharge between scan and sustain electrodes. At this stage, if one lower the potential of address electrode (to the "OFF" level or zero), not it will stop the discharge, but may actually make it stronger.

4. Summary

If a single-scan sub-millisecond addressing of a high-definition (768 lines) panel is achieved, it will remove the time limitations on a number of subfields, and simplify the processing of the image. Combined with a dual-scan method this will also allow the use of ten or more subfields even in the full high-definition panel (1080 lines), and still have less than a millisecond of addressing time per subfield. Having more time for sustaining may result in brighter panels and will simplify the sustain driving.

The proposed addressing scheme may not be as beneficial (in terms of addressing time) in panels utilizing short sustain gap and large plate gap (mostly used today), as in those with wider gap between sustain electrodes and smaller gap between dielectric surfaces above sustain electrodes. The preferred geometry however exhibits higher efficiency and will have significantly smaller jitter than the ones currently used, and thus is more desirable anyway.

This method can be used together with a ramp setup, which is used for a high contrast panels. It may also significantly reduce the cost of the panel, since it requires simpler electronic drivers, and the operating address voltage is low.

5. References

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